REMARKS

The present Amendment amends claims 1, 2, 5, 11, 12, 18 and 28, leaves claims 3, 4, 6-8, 17, 19-27 and 29 unchanged and adds new claims 30-37. Therefore, the present application has pending claims 1-8, 11, 12 and 17-37.

Claims 1, 5, 8, 11, 17, 18, 22, 23, 26 and 27 stand rejected under 35 USC §103(a) as being unpatentable over Tanabe (U.S. Patent No. 5,752,272) in view of Dahlberg (U.S. Patent No. 5,664,169); claims 2, 19 and 20 stand rejected under 35 USC §103(a) as being unpatentable over Tanabe and Dahlberg in view of Genduso (U.S. Patent No. 5,778,422); claims 3, 4 and 21 stand rejected under 35 USC §103(a) as being unpatentable over Tanabe, Dahlberg and further in view of Conary (U.S. Patent No. 5,935,253); claims 12 and 28 stand rejected under 35 USC §103(a) as being unpatentable over Tanabe, Dahlberg, Genduso, Lynch (U.S. Patent No. 5,829,031) and Handy (the text entitled "The Cache Memory Book"); claims 6 and 24 stand rejected under 35 USC §103(a) as being unpatentable over Tanabe and Dahlberg in view of Suzuki (U.S. Patent No. 5,381,532); and claims 7 and 25 stand rejected under 35 USC §103(a) as being unpatentable over Tanabe and Dahlberg in view of Mirza (U.S. Patent No. 5,357,618). These rejections are traversed for the following reasons. Applicants submit that the features of the present invention as now more clearly recited in the claims are not taught or suggested by Tanabe, Dahlberg, Conary, Genduso, Lynch, Handy, Suzuki and Mirza whether taken individually or in combination with each other as suggested by the Examiner. Therefore, Applicants respectfully request the Examiner to reconsider and withdraw

these rejections.

Amendments were made to the claims so as to more clearly recite that the present invention is directed to an information processing system having a processor which includes an internal cache, a memory, a memory controller, a system bus connecting the processor and the memory controller and at least two memory buses connecting the memory controller and the memory. The two memory buses includes a first memory bus for transferring an instruction code to be executed by the processor from the memory to the memory controller and a second memory bus for transferring operand data to be processed by the processor during execution of instruction codes from the memory to the memory controller.

The memory controller includes a buffer, a control circuit and an access judging circuit. The control circuit estimates a most probable address to be accessed next in the memory and the access judging circuit prefetches data stored in the most probable address of the memory into the buffer.

The above described features of the present invention now more clearly recited in the claims are not taught or suggested by any of the references of record particularly Tanabe, Dahlberg, Conary, Genduso, Lynch, Handy, Suzuki or Mirza whether taken individually or in combination with each other as suggested by the Examiner.

As per the Office Action, the Examiner alleges that Tanabe teaches a "micro-processor 3 including built-in cache 3a" corresponds to "a processor having an internal cache" of the present invention, Tanabe's "memory access control device 1" corresponds to "memory controller" of the present invention, Tanabe's "R-DRAM 5"

corresponds to "a memory" of the present invention, Tanabe's "bus control line BC and address line A" corresponds to "system bus" of this invention, Tanabe's "prefetch request unit 21" corresponds to "a control unit" of the present invention, and Tanabe's "control unit 30" corresponds to "an access judging circuit" of the present invention.

Further, in the Office Action, the Examiner alleges that Tanabe's "Rambus line Rb" connecting "memory access control device 1" and "R-DRAM" is a first memory bus, while, Tanabe's "memory bus" connecting "memory controller" and "memory" is at least two a second memory bus corresponding to the present invention.

The above described elements of Tanabe do not correspond to the specific features recited in the claims regarding the at least two memory buses connecting the memory controller and the memory wherein a first bus transfers an instruction code to be executed by the process from the memory to the memory controller and a second memory bus transfer operand data to be processed by the processor during execution of instruction codes from the memory to the memory controller as recited in the claims.

Therefore, Tanabe fails to teach or suggest at least two memory buses connecting the memory controller and the memory wherein the at least two memory buses includes a first memory bus for transferring an instruction code to be executed by the processor from the memory to the memory controller and a second memory bus for transferring operand data to be processed by the processor during execution of instruction codes from the memory to the memory controller as recited in the claims.

The above described deficiencies of Tanabe are not supplied by any of the other references of record particularly Dahlberg, Genduso, Conary, Lynch, Handy, Suzuki or Mirza whether taken individually or in combination with each other as suggested by the Examiner. Therefore, combining the teachings of Tanabe with one or more of Dahlberg, Genduso, Conary, Lyncy, Handy, Suzuki or Mirza as suggested by the Examiner in the Office Action still fails to teach or suggest the features of the present invention as now more clearly recited in the claims.

Dahlberg discloses to access microinstructions from internal control store 278 and data from external control memory 266 at the same time. Dahlberg's "internal control store 278" corresponds to "internal cache" of the present invention and Dahlberg's "external control memory 266" corresponds to "memory" of the present invention. In addition, Dahlberg's "micro sequencer 250" corresponds to an "internal core of a processor" (not clearly disclosed in claims). That is, Dahlberg discloses to access microinstructions from internal control store 278 in the processor (above dotted line in FIG.4) and data from external control memory 266 outside the processor, at the same time.

However, Dahlberg, the same as Tanabe, does not teach or suggest at least two memory buses connecting said memory controller and said memory of the present invention as recited in the claims.

The Examiner asserts in the Office Action that Dahlberg discloses "a first memory bus for transferring an instruction code from the memory to the processor to be executed by the processor and a second bus for transferring operand data from the memory to processor to be processed by the processor during execution of

instruction codes". However, as shown above, Dahlberg discloses a bus for connecting internal control store 278 within the processor (above dotted line in FIG.4) and micro sequencer 250, and a bus for connecting external control memory 266 outside the processor and micro sequencer 250 within the processor. In the present invention, both of the first memory bus and second memory bus connect the memory controller and the memory outside processor. Such features are clearly not taught or suggested by Dahlberg.

Accordingly, Dahlberg fails to teach or suggest a first memory bus for transferring an instruction code to be executed by said processor from said memory to said memory controller, and a second memory bus for transferring operand data to be processed by said processor during execution of instruction codes from said memory to said memory controller of the present invention as recited in the claims.

Further, by combining Tanabe and Dahlberg, the combined apparatus becomes an apparatus in which microinstructions from Tanabe's built-in cache 3a and data from Tanabe's R-DRAM 5 are accessed at the same time. Accordingly, even by combining Tanabe with Dahlberg, the combined apparatus still fails to teach or suggest at least two memory busses connecting said memory controller and said memory of the present invention as recited in the claims.

Genduso merely teaches a structure having only one data path from memory controller to memory. Therefore, in Genduso when conducting a look-ahead operation, such operation obstructs ordinal read/write of data. In the present invention, since two data paths for the memory and memory controller are provided and these two data paths are independently usable for instruction and data, look-

ahead operation does not obstruct ordinal read/write contrary to that taught by Genduso.

Conary discloses look-ahead means as alleged by the Examiner. However, this look-ahead means is located between primary cache and an instruction decoder within microprocessor, and therefore, it is substantially different from the present invention as recited in the claims which is directed to the structure associated with memory controller wherein the first and second memory buses connect the memory and the memory controller to each other.

Lynch discloses an instruction cache and data cache within a microprocessor. That is, Lynch discloses to dispose an independent storing region for each instruction and data in the microprocessor separately. While Lynch is concerned to some extent a memory controller, the features taught therein are substantially different from the features of the present invention as recited in the claims. Furthermore, the operations of a look-ahead buffer and a cache memory are quite different from each other particularly as to whether change of data is permitted or not. A cache must carefully control changes to the data. Thus, Lynch does not supply the above noted deficiencies of Tanabe, Dahlberg, Genduso and Conary.

Handy discloses a kind of textbook for cache memory, and as such suffers from the same deficiencies as Lynch.

Suzuki is concerned with branch estimation. Suzuki was merely cited for claims in which a part of the function of a microprocessor is transplanted to a memory controller. However, as well understood by those of ordinary skill in the art a microprocessor and memory controller are not equivalent to each other. Further, the

transplanted features as taught by Suzuki are not equivalent to the above described features of the present invention as recited in the claims regarding the two memory buses connecting the memory and memory controller. Thus, Suzuki does not supply the above noted deficiencies of Tanabe, Dahlberg, Genduso, Conary, Lynch and Handy.

Mirza discloses to carry out look-ahead of instruction/data with assistance of a compiler. Mirza is quite different from the present invention in that microprocessor controls look-ahead not the memory controller as in the present invention as recited in the claims.

Thus, as is quite clear from the above, the features of the present invention as now more clearly recited in the claims are not taught or suggested by Tanabe, Dahlberg, Genduso, Conary, Handy, Lynch, Suzuki and Mirza whether taken individually or in combination with each other as suggested by the Examiner. Therefore, reconsideration and withdrawal of the above described rejections of the claims under 35 USC §103(a) as being unpatentable over Tanabe in combination with one or more of Dahlberg, Genduso, Conary, Handy, Lynch, Suzuki and Mirza.

The remaining references of record have been studied. Applicants submit that they do not supply any of the deficiencies noted above with respect to the references utilized in the rejection of claims 1-8, 11, 12 and 17-29.

As indicated above, the present Amendment adds new claims 30-37. New claims 30-37 depend respectively from claims 1, 6, 18 and 24. Thus, the same arguments presented above with respect to claims 1, 6, 18 and 24 apply as well to new claims 30-37. Therefore, Applicants submit that the features of the present

invention as recited in new claims 30-37 are not taught or suggested by Tanabe, Dahlberg, Genduso, Conary, Lynch, Handy, Suzuki and Mirza whether taken individually or in combination with each other as suggested by the Examiner.

In view of the foregoing amendments and remarks, applicants submit that claims 1-8, 11, 12 and 17-37 are in condition for allowance. Accordingly, early allowance of claims 1-8, 11, 12 and 17-37 is respectfully requested.

To the extent necessary, the applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, or credit any overpayment of fees, to the deposit account of MATTINGLY, STANGER, MALUR & BRUNDIDGE, P.C., Deposit Account No. 50-1417 (500.36683CX1).

Respectfully submitted,

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